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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Stephen T. Neal
Blakely, Sokoloff, Taylor & Zafman LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1030

EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

4

Office Action Summary	Application No.	Applicant(s)	
	09/940,299	WENDORF ET AL.	
	Examiner	Art Unit	
	John J Tabone, Jr.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/15/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) *10,11,17,24,25,32,33,38,39,45,46 and 49-53* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 12-16,18-23, 26-31, 34-37, 40-44, 47, 48, and 54-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The pending claims 1-9, 12-16,18-23, 26-31, 34-37, 40-44, 47, 48, and 54-57 have been examined.

Drawings

2. The proposed drawing corrections have been received on 3/15/04 and are corrected for the lack of reference signs (Fig. 3) and incorrect labeling (Fig. 4). The objections per paper 2 ¶s 2 and 3 are withdrawn.

Specification

3. The specification objection for inconsistency regarding the "bus slave controller" and signal 328 and the labeling of "memory controller 270" has been corrected and overcome by the applicant. The objections per paper 2 ¶s 4-8 are withdrawn.

Claim Rejections - 35 USC § 112

4. The rejections of claims 10, 11, 24, 25, 38, 39 52, 53 rejected under 35 USC § 112, first paragraph, per paper 2, ¶ 9 have been overcome by the Applicant by canceling these claims. The rejections have been withdrawn.

5. The rejections of claims 2, 4, 11, 17, 25, 31, 39, and 53 rejected under 35 USC § 112, second paragraph, per paper 2 ¶ 10 have been overcome by the Applicant by

amending claims 2, 4, and 31 and canceling claims 11, 17, 25, 39, and 53. The rejections have been withdrawn.

Response to Arguments

Applicant's arguments with respect to claims 1, 16, 30, and 44 have been considered but are moot in view of the new ground(s) of rejection.

Claim1:

The Applicant states that Miner not other prior art cited by the Examiner disclose a bus connecting the processor to the bus slave controller (BSC), wherein the BSC provides access to the memories and that the processor controls the memory test engine (MTE) via the bus and the bus slave controller. The Examiner asserts that Miner teaches the limitation cited in amended claim 1 in that the test execution logic 560 (MTE) directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed (MTE to execute test operations on the memory). Miner also teaches the test management logic 570 (BSC) communicates with a test controller 580 (processor) over the test control bus 575 (bus connecting processor to BSC). Miner also teaches the test management logic 570 (BSC) interfaces to test execution logic 560 (MTE) via bus 574. It is the Examiner's conclusion that claim 1 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Therefore, the rejection is maintained.

Claim 16:

The Applicant states that the amended claim to recite a method for accessing and testing using separate bus slave controllers (BSC) and separate memory test engine (MTE). The Applicant also states that Miner does not teach or suggest such a method. The Examiner asserts that Miner does teach such a method in that test management logic 570 (BSC) receives test parameters (initiation signals) from the test controller 580 (processor) to execute access to any memory (accessing memories) via the test execution logic 560 (MTE) via bus 574. (Col. 10, lines 44-54). The Examiner kindly disagrees that Miner does not teach accessing a plurality of memories. By observing Figure 5 from Miner and Figure 2 from the instance application, one will see that the Applicant illustrates a single BSC and MTE accessing a plurality of memories and this configuration is repeated. Miner teaches a similar configuration. Also, it would be obvious to one skilled in the art to repeat the configuration in Figure 5 of Miner to arrive at the Applicant's invention. It is the Examiner's conclusion that claim 16 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1).

Claim 30:

The Applicant states that Miner does not teach or suggest a capability for accessing a memory via a bus slave controller over a bus, and configuring the memory test engine (MTE) by writing the bus slave controller over the bus. The Examiner asserts, however, that Miner teaches the use of a ROM 571 (machine-readable medium) for storing sequences of microinstructions and passes them from the test controller 580 (processor). Miner further discloses the test management logic 570 (bus

slave controller) inserts operands into the sequence of micro instructions to form a specific sequence and then transfers the specific sequence to the test execution logic 560 (MTE) via bus 574 for perform memory testing (configuring a MTE). (See Col. 11, lines 5-20). Miner also teaches the test execution logic 560 (MTE) compares actual data obtained on a read with the expected data pattern and passes the result of each read to the test management logic 570 (bus slave controller) (processing a signal from the MTE). (Col. 11, lines 26-30). It is the Examiner's conclusion that claim 30 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Therefore, the rejection is maintained.

Claim 44:

The Applicant has rewritten claim 44 to recite a means for simultaneously testing each of a plurality of memories, means for initiating the testing, and means for giving the initiation means access to each of the memories. The Examiners asserts that Miner does teach these means in that the test management logic 570 (MTE and bus slave controller) communicates with a test controller 580 (CPU, means for testing) over the test control bus 575. The test execution logic 560 (MTE, means for testing the memories) directly interfaces to the bus controller 530, the test management logic 570 and the memories 510, thereby allowing the memories 510 to be tested. (See col. 10, lines 8-15). It is the Examiner's conclusion that claim 44 as amended is not patentably distinct or non-obvious over the prior art of record in view of Miner (US-6370661 B1). Therefore, the rejection is maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) The invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 4, 5-8, 12, 13, 30, 34-36, 40, 41, 44, 47, 48, 54, 55 are rejected under 35 U.S.C. 102(b) as being anticipated by Miner (US-6370661 B1).

Claim1:

Miner teaches the limitation cited in amended claim 1 in that the test execution logic 560 (MTE) directly interfaces to the memories 510 and to the bus controller 530, thereby allowing the memories 510 to be tested at full speed (MTE to execute test operations on the memory). Miner also teaches the test management logic 570 (BSC) communicates with a test controller 580 (processor) over the test control bus 575 (bus connecting processor to BSC). Miner also teaches the test management logic 570 (BSC) interfaces to test execution logic 560 (MTE) via bus 574.

Claim 30:

Miner teaches the use of a ROM 571 (machine-readable medium) for storing sequences of microinstructions and passes them from the test controller 580 (processor). Miner further discloses the test management logic 570 (bus slave controller) inserts operands into the sequence of micro instructions to form a specific sequence and then transfers the specific sequence to the test execution logic 560 (MTE) via bus 574 for perform memory testing (configuring a MTE). (See Col. 11, lines

5-20). Miner also teaches the test execution logic 560 (MTE) compares actual data obtained on a read with the expected data pattern and passes the result of each read to the test management logic 570 (bus slave controller) (processing a signal from the MTE). (Col. 11, lines 26-30).

Claim 44:

Miner teaches the means limitations in the amended claim 44 in that the test management logic 570 (MTE and bus slave controller) communicates with a test controller 580 (CPU, means for testing) over the test control bus 575. Miner also teaches the test execution logic 560 (MTE, means for testing the memories) directly interfaces to the bus controller 530, the test management logic 570 and the memories 510, thereby allowing the memories 510 to be tested. (See col. 10, lines 8-15).

Claims 4, 5-8, 12, 13, 34-36, 40, 41, 47, 48, 54, 55:

See paper no. 2 (mailed 12/12/03) for detail of prior rejections.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 9, 15, 16, 19-23, 25-27, 29, 31, 37, 39, 43, and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1).

Claim 16:

Miner teaches that test management logic 570 (bus slave controller (BSC)) receives test parameters (initiation signals) from the test controller 580 (processor) to execute access to any memory (accessing memories) via the test execution logic 560 (MTE) via bus 574. (Col. 10, lines 44-54). Miner teaches in Figure 5 a single BSC and MTE accessing a plurality of memories. It would have been obvious to one of ordinary skill in the art at the time the invention was made to repeat Miner's test management logic 570 (BSC) and test execution logic 560 (MTE) in Figure 5. The artisan would have been motivated to do so because it would enable Miner to test multiple banks of memories.

Claim 19:

Miner teaches the test execution logic 560 executes test sequences of data patterns to write and expected data patterns to read. (See col. 10, lines 49-54, col. 11, lines 12-18).

Claim 20:

Miner teaches the test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 27-29).

Claim 21:

Miner teaches the test sequences that are designed into the test management logic 570 can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. In addition, a test sequence can be configured to repeat a specified number of times before it completes. (See col. 10, lines 49-56). Miner also teaches the

test execution logic 560 compares actual data obtained on a read with the expected data pattern on a bit-by-bit basis. (See col. 11, lines 26-28).

Claim 22:

Miner teaches the test execution logic 560 generates addresses for specified locations in a memory. Miner also teaches the test sequences within the test management logic 570 are configurable, and they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. (See col. 10, lines 31, 32, 45-54). Miner also teaches that the test execution logic 560 executes test parameters consisting of variables to prescribe a designated memory 510 for testing, start address, address increment amount, data pattern to write, expected data pattern on a read... (See col. 11, lines 10 –18).

Claims 26 and 27:

Miner teaches that the result of each read, containing a bit-by-bit result, is provided to the test management logic 570 via bus 574. The result is placed in the result register 573 for retrieval by the test controller 580. (See col. 11, lines 28-31 and col. 10, lines 56-60).

Claims 2, 9, 15, 23, 29, 31, 37, 39, 43, and 57:

See paper no. 2 (mailed 12/12/03) for detail of prior rejections.

8. Claims 3, 18, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Satoh (US-6501690 B2).

Claims 3, 18, and 32:

See paper no. 2 (mailed 12/12/03) for detail of prior rejections.

9. Claims 14, 28, 42, 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miner (US-6370661 B1) and further in view of Chambers et al. (US-20020078408 A1).

Claims 14, 28, 42, 56:

See paper no. 2 (mailed 12/12/03) for detail of prior rejections.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJT

CHRISTINE T. TU
Primary Examiner